What is claimed is:

1. A method for forming a semiconductor device, comprising:

forming a first pattern for a semiconductor device in a semiconductor device formation region of a semiconductor substrate and simultaneously forming the first pattern in a first mark formation region of the semiconductor substrate;

forming a second pattern for the semiconductor device on a resultant structure in the semiconductor device formation region of the semiconductor substrate and simultaneously forming the second pattern in a second mark formation region of the semiconductor substrate; and

inspecting the first pattern in the first mark formation region and the second pattern in the second mark formation region for misalignments.

2. The method for forming a semiconductor device as claimed in claim 1, wherein the first mark formation region is a box shaped main scale formation region, and the second mark formation region is a box shaped vernier formation region.

3. The method for forming a semiconductor device as claimed in claim 2, wherein the first pattern is an active pattern in a DRAM cell region, and the second pattern is a word line pattern in the DRAM cell region.

4. The method for forming a semiconductor device as claimed in claim 1, wherein a scattering bar is formed at an edge of a pattern in a mask corresponding to the first pattern in the first mark formation region.

5. The method for forming a semiconductor device as claimed in claim 1, wherein a scattering bar is formed at an edge of a pattern in a mask corresponding to the second pattern in the second mark formation region.

6. A semiconductor device having an overlay mark, the overlay mark, comprising:

a first mark formed in a first mark formation region of a semiconductor substrate and a first pattern formed in a semiconductor device formation region of the semiconductor substrate, wherein the first mark and the first pattern are formed simultaneously by a same process such that the first mark has a shape identical to a shape of the first pattern; and

a second mark formed in a second mark formation region of the semiconductor substrate and a second pattern formed in the semiconductor device formation region of the semiconductor substrate, wherein the second mark and the second pattern are formed simultaneously by a same process such that the second mark has a shape identical to a shape of the second pattern.

7. The semiconductor device as claimed in claim 6, wherein the first mark formation region is a box shaped main scale formation region, and the second mark formation region is a box shaped vernier formation region.

8. The semiconductor device as claimed in claim 7, wherein the first pattern is an active pattern in a DRAM cell region, and the second pattern is a word line pattern in the DRAM cell region.